Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	13941	((709/203) or (709/204-211) or (709/212-213) or (709/213) or (709/238) or (711/146) or (711/117-146) or (711/147) or (711/167) or (712/10) or (712/32) or (712/203) or (712/245) or (370/211)).CCLS.	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/04/15 21:54
S2	111524	(("709") or ("710") or ("711") or ("712") or ("370")).CLAS.	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/04/15 21:55
S3	462	(allen adj james).inv.	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/04/15 21:55
S4	4	(allen adj james).inv. and snoop$3	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/04/15 21:55
S5	51	("4325085" | "4494108" | "4929946" | "4973961" | "5014134" | "5097261" | "5109226" | "5138315" | "5225832" | "5272478" | "5276525" | "5302949" | "5313203" | "5319457" | "5357250").PN. OR ("5717394"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/04/15 21:58
S6	210798	("4325085" | "4494108" | "4929946" | "4973961" | "5014134" | "5097261" | "5109226" | "5138315" | "5225832" | "5272478" | "5276525" | "5302949" | "5313203" | "5319457" | "5357250").PN. OR ("5717394"). URPN. ans multiprocessor	US-PGPUB; USPAT; USOCR	OR	OFF	2005/04/15 21:58
S7	19	("4325085" | "4494108" | "4929946" | "4973961" | "5014134" | "5097261" | "5109226" | "5138315" | "5225832" | "5272478" | "5276525" | "5302949" | "5313203" | "5319457" | "5357250").PN. OR ("5717394"). URPN. and multiprocessor	US-PGPUB; USPAT; USOCR	OR	OFF	2005/04/15 21:58

S8	15	("4325085" | "4494108" | "4929946" | "4973961" | "5014134" | "5097261" | "5109226" | "5138315" | "5225832" | "5272478" | "5276525" | "5302949" | "5313203" | "5319457" | "5357250").PN. OR ("5717394"). URPN. and multiprocessor and snoop$3	US-PGPUB; USPAT; USOCR	OR	OFF	2005/04/15 21:59
S9	1817	multiprocessor and snoop$3	US-PGPUB; USPAT; USOCR	OR	OFF	2005/04/15 22:00
S10	1023	(multiprocessor and snoop$3)same bus$2	US-PGPUB; USPAT; USOCR	OR	OFF	2005/04/15 22:01
S11	14023	(multiprocessor same system)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/04/15 22:02
S12	19551	((multiprocessor or (multi adj processor) or multi-processor) same system)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/04/15 22:03
S13	1367	((multiprocessor or (multi adj processor) or multi-processor) same system) same logic	US-PGPUB; USPAT; USOCR	OR	OFF	2005/04/15 22:03
S14	315	(((multiprocessor or (multi adj processor) or multi-processor) same system) same logic same interface$3)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/04/15 22:03
S15	316	(((multiprocessor or (multi adj processor) or multi-processor) same system) same logic same interfac$3) and (microprocessor or processor)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/04/15 22:04
S16	336	(((multiprocessor or (multi adj processor) or multi-processor) same system) same logic same interfac$3) and (microprocessor or processor)	US-PGPUB; USPAT; USOCR	OR	ON	2005/04/15 22:05
S17	173	(((multiprocessor or (multi adj processor) or multi-processor) same system) same logic same interfac$3) and ((microprocessor or processor) same clock)	US-PGPUB; USPAT; USOCR	OR	ON	2005/04/15 22:05
S18	151	(((multiprocessor or (multi adj processor) or multi-processor) same system) same logic same interfac$3) and ((microprocessor or processor) same clock) and ((microprocessor or processor) same first)	US-PGPUB; USPAT; USOCR	OR	ON	2005/04/15 22:06

S19	142	(((multiprocessor or (multi adj processor) or multi-processor) same system) same logic same interfac$3) and ((microprocessor or processor) same clock) and ((microprocessor or processor) same first) and ((microprocessor or processor) same second)	US-PGPUB; USPAT; USOCR	OR	ON	2005/04/15 22:06
S20	86	(((multiprocessor or (multi adj processor) or multi-processor) same system) same logic same interfac$3) and ((microprocessor or processor) same clock) and ((microprocessor or processor) same first) and ((microprocessor or processor) same second) and ((microprocessor or processor) same third)	US-PGPUB; USPAT; USOCR	OR	ON	2005/04/15 22:06
S21	36	(((multiprocessor or (multi adj processor) or multi-processor) same system) same logic same interfac$3) and ((microprocessor or processor) same clock) and ((microprocessor or processor) same first) and ((microprocessor or processor) same second) and ((microprocessor or processor) same third) and ((microprocessor or processor) same fourth)	US-PGPUB; USPAT; USOCR	OR	ON	2005/04/15 22:06
S22	14	(((multiprocessor or (multi adj processor) or multi-processor) same system) same logic same interfac$3) and ((microprocessor or processor) same clock) and ((microprocessor or processor) same first) and ((microprocessor or processor) same second) and ((microprocessor or processor) same third) and ((microprocessor or processor) same fourth) and ((microprocessor or processor) same fifth)	US-PGPUB; USPAT; USOCR	OR	ON	2005/04/15 22:07

S23	9	(((multiprocessor or (multi adj processor) or multi-processor) same system) same logic same interfac$3 same bus) and ((microprocessor or processor) same clock) and ((microprocessor or processor) same first) and ((microprocessor or processor) same second) and ((microprocessor or processor) same third) and ((microprocessor or processor) same fourth) and ((microprocessor or processor) same fifth)	US-PGPUB; USPAT; USOCR	OR	ON	2005/04/15 22:18
S24	103	(((multiprocessor or (multi adj processor) or multi-processor) same system) same logic same interfac$3 same bus) and ((microprocessor or processor) same clock)	US-PGPUB; USPAT; USOCR	OR	ON	2005/04/15 22:19
S25	58	(((multiprocessor or (multi adj processor) or multi-processor) same system) same logic same interfac$3 same bus) and ((microprocessor or processor) same clock) and multiplex$3	US-PGPUB; USPAT; USOCR	OR	ON	2005/04/15 22:19
S26	38	(((multiprocessor or (multi adj processor) or multi-processor) same system) same logic same interfac$3 same bus) and ((microprocessor or processor) same clock) and multiplex$3 and delay	US-PGPUB; USPAT; USOCR	OR	ON	2005/04/15 22:19
S27	37	(((multiprocessor or (multi adj processor) or multi-processor) same system) same logic same interfac$3 same bus) and ((microprocessor or processor) same clock) and multiplex$3 and delay and (data with buses)	US-PGPUB; USPAT; USOCR	OR	ON	2005/04/15 22:20
S28	31	(((multiprocessor or (multi adj processor) or multi-processor) same system) same logic same interfac$3 same bus) and ((microprocessor or processor) same clock) and multiplex$3 and delay and (data with buses with signal)	US-PGPUB; USPAT; USOCR	OR	ON	2005/04/15 22:20

S29	29	(((multiprocessor or (multi adj processor) or multi-processor) same system) same logic same interfac$3 same bus) and ((microprocessor or processor) same clock same memor$3) and multiplex$3 and delay and (data with buses with signal)	US-PGPUB; USPAT; USOCR	OR	ON	2005/04/15 22:21
S30	12	(((multiprocessor or (multi adj processor) or multi-processor) same system) same logic same interfac$3 same bus) and ((microprocessor or processor) same clock same memor$3) and multiplex$3 and delay and (data with buses with signal) and (receiv$3 same signal same data same time)	US-PGPUB; USPAT; USOCR	OR	ON	2005/04/17 23:42
S31	1	(((multiprocessor or (multi adj processor) or multi-processor) same system) same logic same interfac$3 same bus) and ((microprocessor or processor) same clock same memor$3) and (multiplex$3 same delay same (data with buses with signal)) and (receiv$3 same signal same data same time)	US-PGPUB; USPAT; USOCR	OR	ON	2005/04/15 22:23
S32	12	(((multiprocessor or (multi adj processor) or multi-processor) same system) same logic same interfac$3 same bus) and ((microprocessor or processor) same clock same memor$3) and multiplex$3 and delay and (data with buses with signal) and (receiv$3 same signal same data same time)	US-PGPUB; USPAT; USOCR	OR	ON	2005/04/17 23:42
S33	1	(((multiprocessor or (multi adj processor) or multi-processor) same system) same logic same interfac$3 same bus) and ((microprocessor or processor) same clock same memor$3) and multiplex$3 and delay and (data with buses with signal) and (receiv$3 same signal same data same time) and "709".clss.	US-PGPUB; USPAT; USOCR	OR	ON	2005/04/17 23:43

S34	0	(((multiprocessor or (multi adj processor) or multi-processor) same system) same logic same interfac$3 same bus) and ((microprocessor or processor) same clock same memor$3) and multiplex$3 and delay and (data with buses with signal) and (receiv$3 same signal same data same time) and "711".clss.	US-PGPUB; USPAT; USOCR	OR	ON	2005/04/17 23:44
S35	0	(((multiprocessor or (multi adj processor) or multi-processor) same system) same logic same interfac$3 same bus) and ((microprocessor or processor) same clock same memor$3) and multiplex$3 and delay and (data with buses with signal) and (receiv$3 same signal same data same time) and "712".clss.	US-PGPUB; USPAT; USOCR	OR	ON	2005/04/17 23:44
S36	0	(((multiprocessor or (multi adj processor) or multi-processor) same system) same logic same interfac$3 same bus) and ((microprocessor or processor) same clock same memor$3) and multiplex$3 and delay and (data with buses with signal) and (receiv$3 same signal same data same time) and "370".clss.	US-PGPUB; USPAT; USOCR	OR	ON	2005/04/17 23:44
S37	2	"5555382".pn.	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/10/10 19:12
S38	2	"6754838".pn.	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/10/10 19:18
S39	10533	processor with connect$3 with memory with bus	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/10/10 19:18
S40	639	(processor with connect$3 with memory with bus) same clock	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/10/10 19:19
S41	729	(processor with connect$3 with memory with bus) same clock	USPAT; EPO; JPO; DERWENT	OR	ON	2005/10/10 19:19
S42	261	((processor with connect$3 with memory with bus) same clock) and (first near5 clock)	USPAT; EPO; JPO; DERWENT	OR	ON	2005/10/10 19:20
S43	191	((processor with connect$3 with memory with bus) same clock) and (first near5 clock) and ((second or another) near5 clock)	USPAT; EPO; JPO; DERWENT	OR	ON	2005/10/10 19:20

S44	79	((processor with connect$3 with memory with bus) same clock) and (first near5 clock) and ((second or another) near5 clock) and (first near5 processor)	USPAT; EPO; JPO; DERWENT	OR	ON	2005/10/10 19:20
S45	61	((processor with connect$3 with memory with bus) same clock) and (first near5 clock) and ((second or another) near5 clock) and (first near5 processor)and ((second or another) near5 processor)	USPAT; EPO; JPO; DERWENT	OR	ON	2005/10/10 19:21
S46	47	((processor with connect$3 with memory with bus) same clock) and (first near5 clock) and ((second or another) near5 clock) and (first near5 processor)and ((second or another) near5 processor) and (first near5 signal)	USPAT; EPO; JPO; DERWENT	OR	ON	2005/10/10 19:21
S47	45	((processor with connect$3 with memory with bus) same clock) and (first near5 clock) and ((second or another) near5 clock) and (first near5 processor)and ((second or another) near5 processor) and (first near5 signal)and ((second or another) near5 signal)	USPAT; EPO; JPO; DERWENT	OR	ON	2005/10/10 19:21
S48	39	((processor with connect$3 with memory with bus) same clock) and (first near5 clock) and ((second or another) near5 clock) and (first near5 processor)and ((second or another) near5 processor) and ((first near5 signal)same ((second or another) near5 signal))	USPAT; EPO; JPO; DERWENT	OR	ON	2005/10/10 19:22
S49	33	((processor with connect$3 with memory with bus) same clock) and (first near5 clock) and ((second or another) near5 clock) and (first near5 processor)and ((second or another) near5 processor) and ((first near5 signal)same ((second or another) near5 signal)) and (first near5 bus)	USPAT; EPO; JPO; DERWENT	OR	ON	2005/10/10 19:23

S50	26	((processor with connect$3 with memory with bus) same clock) and (first near5 clock) and ((second or another) near5 clock) and (first near5 processor)and ((second or another) near5 processor) and ((first near5 signal)same ((second or another) near5 signal)) and (first near5 bus)same ((second or another)near5 bus)	USPAT; EPO; JPO; DERWENT	OR	ON	2005/10/10 19:24
S51	26	((processor with connect$3 with memory with bus) same clock) and (first near5 clock) and ((second or another) near5 clock) and (first near5 processor)and ((second or another) near5 processor) and ((first near5 signal)same ((second or another) near5 signal)) and ((first near5 bus)same ((second or another)near5 bus))	USPAT; EPO; JPO; DERWENT	OR	ON	2005/10/10 19:25
S52	22	((processor with connect$3 with memory with bus) same clock) and (first near5 clock) and ((second or another) near5 clock) and (first near5 processor)and ((second or another) near5 processor) and ((first near5 signal)same ((second or another) near5 signal)) and ((first near5 bus)same ((second or another)near5 bus)) and (memory near5 controller)	USPAT; EPO; JPO; DERWENT	OR	ON	2005/10/10 19:25
S53	0	((processor with connect$3 with memory with bus) same clock) and (first near5 clock) and ((second or another) near5 clock) and (first near5 processor)and ((second or another) near5 processor) and ((first near5 signal)same ((second or another) near5 signal)) and ((first near5 bus)same ((second or another)near5 bus)) and ((memory near5 controller)same multiprocssor)	USPAT; EPO; JPO; DERWENT	OR	ON	2005/10/10 19:25

S54	0	((processor with connect$3 with memory with bus) same clock) and (first near5 clock) and ((second or another) near5 clock) and (first near5 processor)and ((second or another) near5 processor) and ((first near5 signal)same ((second or another) near5 signal)) and ((first near5 bus)same ((second or another)near5 bus)) and ((memory near5 controller)same multiprocessor)	USPAT; EPO; JPO; DERWENT	OR	ON	2005/10/10 19:25
S55	22	((processor with connect$3 with memory with bus) same clock) and (first near5 clock) and ((second or another) near5 clock) and (first near5 processor)and ((second or another) near5 processor) and ((first near5 signal)same ((second or another) near5 signal)) and ((first near5 bus)same ((second or another)near5 bus)) and ((memory near5 controller))	USPAT; EPO; JPO; DERWENT	OR	ON	2005/10/10 19:26
S56	6	((processor with connect$3 with memory with bus) same clock) and (first near5 clock) and ((second or another) near5 clock) and (first near5 processor)and ((second or another) near5 processor) and ((first near5 signal)same ((second or another) near5 signal)) and ((first near5 bus)same ((second or another)near5 bus)) and ((memory near5 controller)) and multiprocessor	USPAT; EPO; JPO; DERWENT	OR	ON	2005/10/10 19:26
S57	6	((processor with connect$3 with memory with bus) same clock) and (first near5 clock) and ((second or another) near5 clock) and (first near5 processor)and ((second or another) near5 processor) and ((first near5 signal)same ((second or another) near5 signal)) and ((first near5 bus)same ((second or another)near5 bus)) and ((memory near5 controller)) and (multiprocessor or multi-processor)	USPAT; EPO; JPO; DERWENT	OR	ON	2005/10/11 14:52

S58	1	((processor with connect$3 with memory with bus) same clock) and (first near5 clock) and ((second or another) near5 clock) and (first near5 processor)and ((second or another) near5 processor) and ((first near5 signal)same ((second or another) near5 signal)) and ((first near5 bus)same ((second or another)near5 bus)) and ((memory near5 controller)) and ((multiprocessor or multi-processor) same response same time)	USPAT; EPO; JPO; DERWENT	OR	ON	2005/10/10 19:27
S59	39	((processor with connect$3 with memory with bus) same clock) and (first near5 clock) and ((second or another) near5 clock) and (first near5 processor)and ((second or another) near5 processor) and ((first near5 signal)same ((second or another) near5 signal))	USPAT; EPO; JPO; DERWENT	OR	ON	2005/10/11 14:53
S60	1	((processor with connect$3 with memory with bus) same clock) and (first near5 clock) and ((second or another) near5 clock) and (first near5 processor)and ((second or another) near5 processor) and ((first near5 signal)same ((second or another) near5 signal)) and ((first near5 bus)same ((second or another)near5 bus)) and ((memory near5 controller)) and (multiprocessor or multi-processor) and (delay$3 near5 signal)	USPAT; EPO; JPO; DERWENT	OR	ON	2005/10/11 14:53